DEPARTMENT OF ELECTRICAL ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY SRINAGAR

Applications are invited from interested candidates for a temporary engagement as a Project Assistant for a research project "Model Order Reduction for Simulation Acceleration in Power Electronics" sponsored by the Central Power Research Institute (CPRI) Bangalore.

Project Details:

Name & No. of Positions	Project Assistant; 01 Post.
Place	Department of Electrical Engineering, National Institute of Technology Srinagar Hazratbal 190006 J&K
Qualification	a) M. E. / M. Tech in relevant fields of Electrical Engineering (minimum CGPA: 8.0 / 80 %), or b) B. E. / B. Tech in Electrical Engineering (minimum CGPA 8.0 / 80%) and a valid GATE score Expertise in MATLAB/Simulink is essential. A thorough understanding of Control Systems, Power Electronics and Linear Algebra is desirable.
Duration	06 – 09 months
Salary	Rs. 25,000/- pm + HRA (likely to be revised to Rs. 31,000/- pm + HRA) as per institute norms. Campus Accommodation is not available.
Commitment	The candidate is expected to commit his/her availability until the completion of the project.
Selection Process	Candidates should e-mail their CVs to the Principal Investigator (PI). Shortlisted candidates will be called foran interview. All relevant documents should be brought along at the time of the test. No TA/DA will be paid for participating in the selection process. The selected candidate is expected to join within a week after intimation of their selection else it wouldbe offered to a candidate in waiting list.
Contact Details	Dr. Mohammad Abid Bazaz Dept. of Electrical Engineering, NIT Srinagar Email: abid@nitsri.net Please include the following details in your CV: i) Marks obtained in Control Systems, Power Electronics and MATLAB courses. ii) GATE Score iii) Rank in class and total class strength iv) Publications/Prizes/Awards if any.

Interested candidates may e-mail their CVs by 22 April 2019.

Sd/=

Registrar