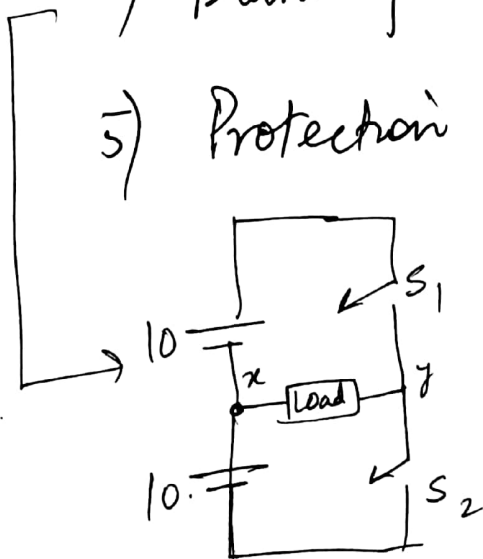


Any device receiving a gate pulse, shall receive it through a gate driver.
(MOSFET IGBT)

DRIVER CIRCUIT. (MOSFETS/IGBTs)

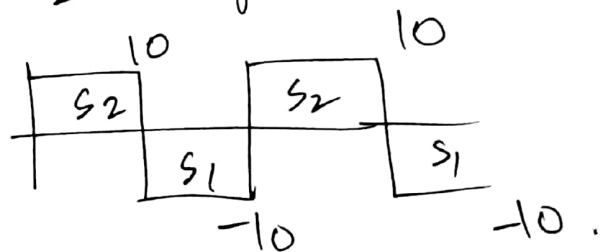
Interface b/w controller & power ckt.

- 1) Pulse Amplification
- 2) Isolation
- 3) Pulse polarity control (Bipolar/unipolar)
- 4) Blanking time
- 5) Protection Against Overcurrents.



$S_1 \Rightarrow V_{xy} = -10$

$S_2 \Rightarrow V_{xy} = 10$

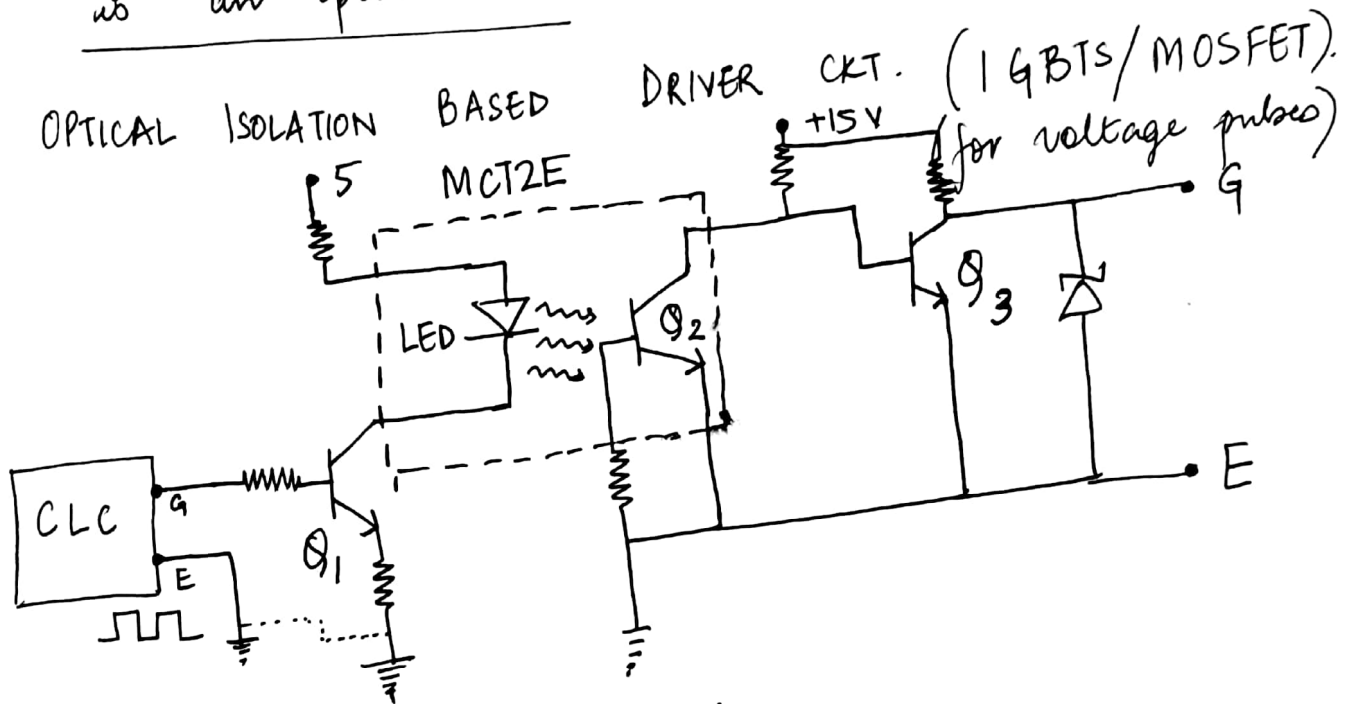


Complementary switches

Overlap possible hence blanking time needed to prevent short ckt

In order to provide electrical isolation, a device ckt may employ any isolation mechanism e.g transformer, optical isolation, bootstrap circuit.

One of the most popular ckt used for gate driving is an optical isolator.



When CLC pulse goes high,

Q_1 receives a base drive.

\rightarrow saturation $\Rightarrow I_c \uparrow \uparrow$.

$\Rightarrow I_c$ flows via LED.

\Rightarrow LED glows.

\Rightarrow Light falls on the base region of Q_2 which is a light activated transistor.

$\Rightarrow Q_2$ goes into saturation due to base drive in the form of light.

$\Rightarrow I_c \uparrow$ of $Q_2 \Rightarrow$ Voltage at Base of Q_3 is zero.

Q_3 does not receive a base drive \Rightarrow hence remains OFF

\therefore 15V appears across GE.

V_{GE} goes high.

~~#~~

When clc pulse goes low,

base drive removed to Q_1 . $\Rightarrow Q_1$ OFF

\Rightarrow LED OFF

$\Rightarrow Q_2$ OFF.

$\Rightarrow Q_3$ receives base drive,

\Rightarrow goes into conduction.

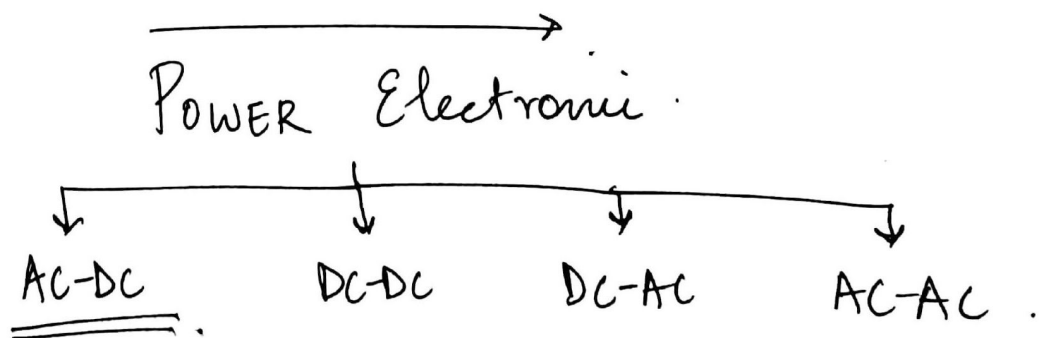
$\Rightarrow V_{GE} = 0$. (pulse goes low).

THIS FINISHES THE

PRE-REQUISITES FOR

STUDYING POWER ELECTRONIC

CIRCUITS.



Practise Set- II
Power Electronics (ELE 603)
 Department of Electrical Engineering
 National Institute of Technology, Srinagar

Course Coordinator: Ms. Tabish Nazir Mir

The following questions are meant for practice purpose. No submission is expected.

1) For the circuit shown in Fig. 1, find out the ratios $N_1 : N_2, N_3 : N_4, N_5 : N_6,$ and $N_7 : N_8$ of the center tapped reactors, such that current is equally shared between the five thyristors, and also between the feeders such that $I_1 = I_2 = I_3 = I_4$.

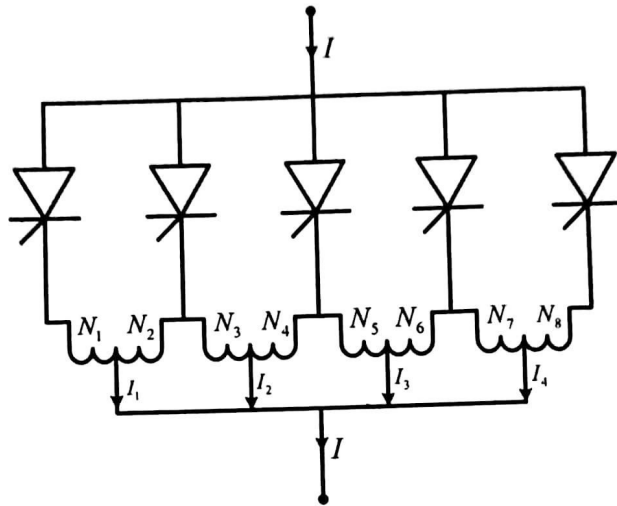


Fig. 1

2) A fully controlled switch is connected in a DC circuit with $V_{DC} = 100V$. The pattern of current flowing through the switch is illustrated in Fig. 2. If the ON-state resistance of the switch is 0.1Ω , find the average ON-state power loss. Assuming there is no other loss in the circuit (i.e no switching power loss and no power loss when the device is OFF), calculate the circuit efficiency.

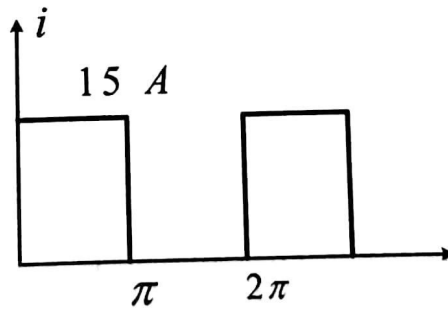


Fig. 2

Q3:) You are trying to design a circuit using thyristors in the Power Electronics Lab. Only four thyristors (T_0, T_1, T_2, T_3) are available to you, each rated at 325V, 30A. The forward blocking resistance of each SCR is $10k\Omega$, $11k\Omega$, $12k\Omega$, and $13k\Omega$ respectively. Your application requires a 900V, 20A thyristor, so you connect three SCRs in series (without any equalizing circuits).

a) Out of four thyristors, the choice of three can be made in ${}^4C_3 = 4$ ways. Out of these 4, two choices are the most optimum. Which two of the four combinations are the most optimum and why? .

b) For the two best combinations, find the voltage shared by each device in each combination.

c) From the two best combinations, can you now choose your final selection? If yes, which one would it be and why?

Q4:) As a design engineer you are expected to design a 12V DC supply for a $10\ \Omega$ load when the input is 50V DC.

a) Your first design is a preliminary one, based on the use of a potential divider. Draw the circuit and calculate its efficiency.

b) You just realised that your design is very poor and you need to incorporate the knowledge of power electronics to design a new circuit. Draw your new circuit design and mention which power electronics device you will use and why?

c) For generating 12V (Average) output from 50 V input, determine the percentage of time for which your device will be ON over one switching cycle.

d) Assume that your device carries a leakage current of 0.01 A when OFF and drops a voltage of 1V when ON. Also assume the switching transitions are instantaneous (Switching loss = 0) and the device is operated at 1kHz. Find the efficiency of your new design.